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Search Results -

Terms	Documents
L1 same (serial adj1 bus)	23

Database: US Patents Full-Text Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

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Search History

DATE: Tuesday, March 11, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	L1 same (serial adj1 bus)	23	L3
L2	L1 same bus	581	L2
L1	configur$5 near5 ROM	2539	L1

END OF SEARCH HISTORY

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Database: US Patents Full-Text Database
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JPO Abstracts Database
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IBM Technical Disclosure Bulletins

Term: l3 same node

Display: 10 **Documents in Display Format:** TI **Starting with Number** 1

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DATE: Tuesday, March 11, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L6	l3 same node	19	L6
L5	L4 same bus	38	L5
L4	L1 same node	71	L4
L3	L1 same (serial adj1 bus)	23	L3
L2	L1 same bus	581	L2
L1	configur$5 near5 ROM	2539	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
((358/1.15)!.CCLS. |(370/463)!.CCLS. |(709/253 |709/301 |709/302 |709/220)!.CCLS. |(710/104 |710/105 |710/106 |710/62 |710/63 |710/2 |710/305 |710/8)!.CCLS. |(714/1)!.CCLS.)	4949

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L7

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Search History

DATE: Tuesday, March 11, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L7	((358/1.15)!.CCLS. |(370/463)!.CCLS. |(709/253 |709/301 |709/302 |709/220)!.CCLS. |(710/104 |710/105 |710/106 |710/62 |710/63 |710/2 |710/305 |710/8)!.CCLS. |(714/1)!.CCLS.)	4949	L7
L6	l3 same node	19	L6
L5	L4 same bus	38	L5
L4	L1 same node	71	L4
L3	L1 same (serial adj1 bus)	23	L3
L2	L1 same bus	581	L2
L1	configur$5 near5 ROM	2539	L1

WEST

Help | Logout | Interrupt

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
l2 and L7	63

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L8

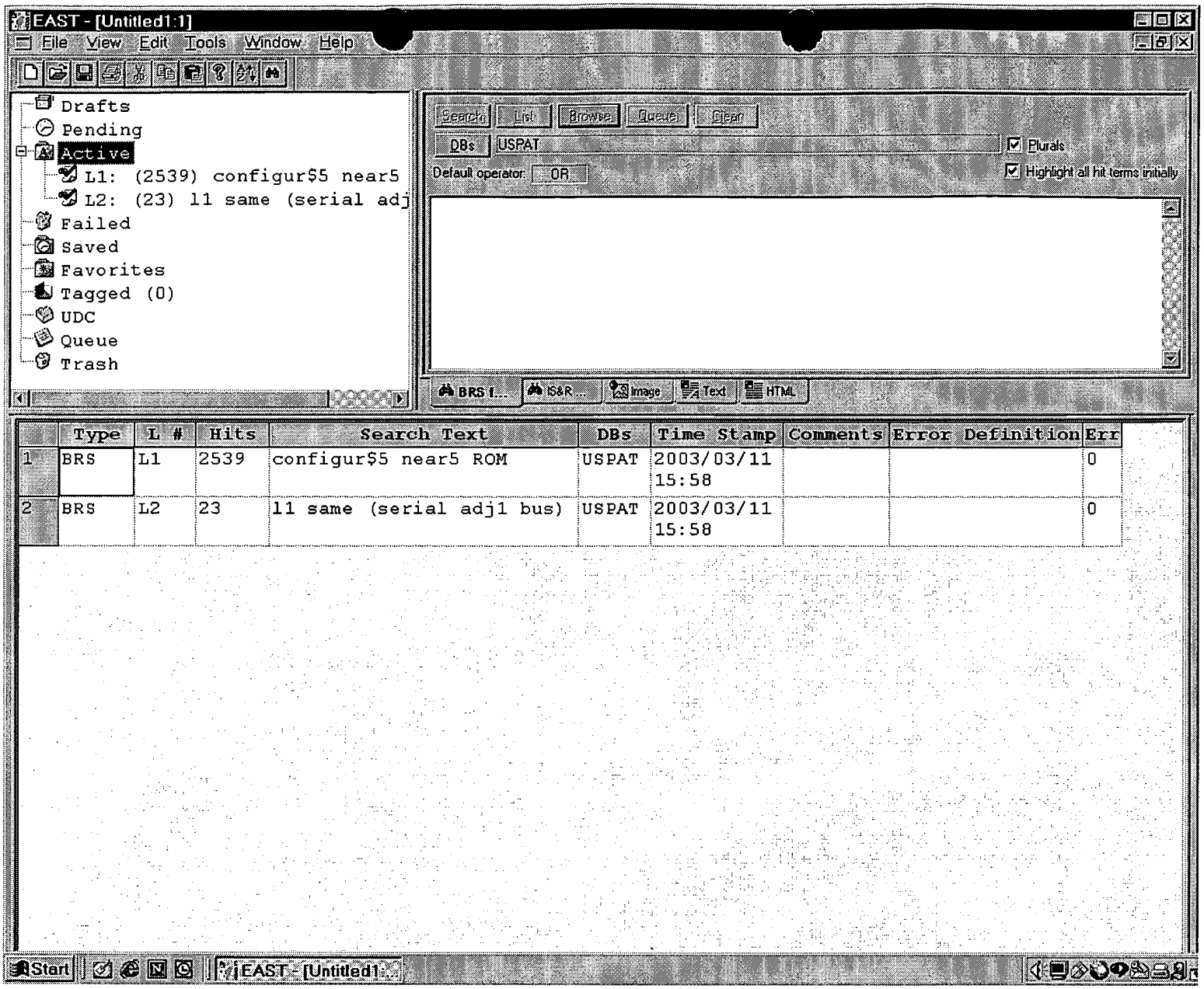
Refine Search

Recall Text | Clear

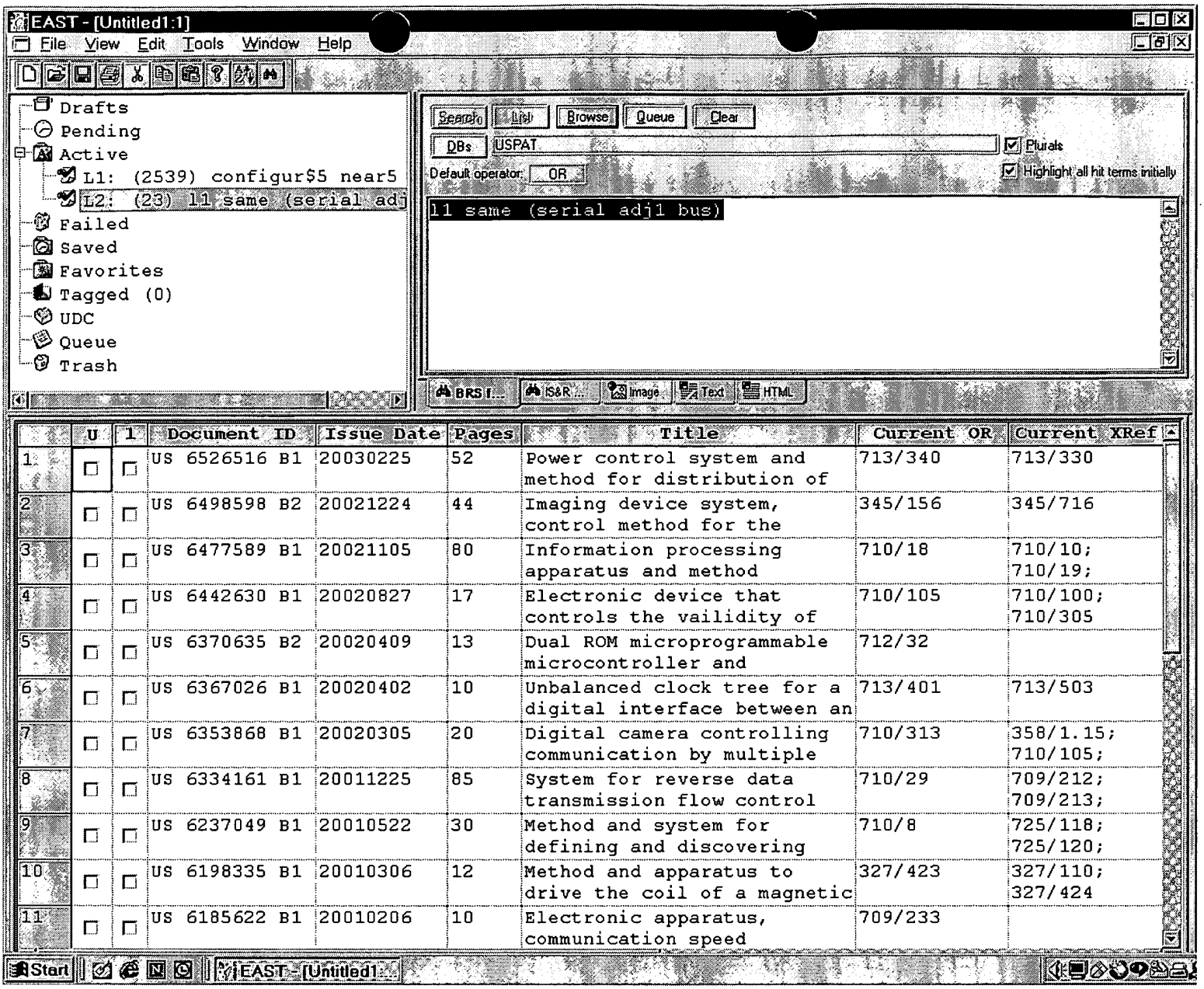
Search History

DATE: Tuesday, March 11, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L8	l2 and L7	63	L8
L7	((358/1.15)!.CCLS. |(370/463)!.CCLS. |(709/253 |709/301 |709/302 |709/220)!.CCLS. |(710/104 |710/105 |710/106 |710/62 |710/63 |710/2 |710/305 |710/8)!.CCLS. |(714/1)!.CCLS.)	4949	L7
L6	l3 same node	19	L6
L5	L4 same bus	38	L5
L4	L1 same node	71	L4
L3	L1 same (serial adj1 bus)	23	L3
L2	L1 same bus	581	L2
L1	configur$5 near5 ROM	2539	L1



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	2539	configur$5 near5 ROM	USPAT	2003/03/11 15:58			0
2	BRS	L2	23	l1 same (serial adj1 bus)	USPAT	2003/03/11 15:58			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6526516 B1	20030225	52	Power control system and method for distribution of	713/340	713/330
2	☐	☐	US 6498598 B2	20021224	44	Imaging device system, control method for the	345/156	345/716
3	☐	☐	US 6477589 B1	20021105	80	Information processing apparatus and method	710/18	710/10; 710/19;
4	☐	☐	US 6442630 B1	20020827	17	Electronic device that controls the vailidity of	710/105	710/100; 710/305
5	☐	☐	US 6370635 B2	20020409	13	Dual ROM microprogrammable microcontroller and	712/32	
6	☐	☐	US 6367026 B1	20020402	10	Unbalanced clock tree for a digital interface between an	713/401	713/503
7	☐	☐	US 6353868 B1	20020305	20	Digital camera controlling communication by multiple	710/313	358/1.15; 710/105;
8	☐	☐	US 6334161 B1	20011225	85	System for reverse data transmission flow control	710/29	709/212; 709/213;
9	☐	☐	US 6237049 B1	20010522	30	Method and system for defining and discovering	710/8	725/118; 725/120;
10	☐	☐	US 6198335 B1	20010306	12	Method and apparatus to drive the coil of a magnetic	327/423	327/110; 327/424
11	☐	☐	US 6185622 B1	20010206	10	Electronic apparatus, communication speed	709/233	

Your search matched **2** of **924782** documents.

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Then click **Search Again.**

(configur* and ROM) and bus

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Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A large scale FPGA with 10 K core cells with CMOS 0.8 μm 3-laye metal process**
Muroga, H.; Murata, H.; Saeki, Y.; Hibi, T.; Ohashi, Y.; Noguchi, T.; Nishimura,
Custom Integrated Circuits Conference, 1991., Proceedings of the IEEE 1991 , May 1991
Page(s): 6.4/1 -6.4/4

[Abstract] [PDF Full-Text (188 KB)] **IEEE CNF**

2 **A reusable microcontroller core's design**
Janiszewki, I.; Baraniecki, R.; Siekierska, K.;
Fall VIUF Workshop, 1999. , Oct 1999
Page(s): 14 -19

[Abstract] [PDF Full-Text (636 KB)] **IEEE CNF**

A reusable microcontroller core's design

Janiszewki, I. Baraniecki, R. Siekierska, K.
Inst. of Electron Technol., Warsaw;

This paper appears in: **Fall VIUF Workshop, 1999.**
10/04/1999 -10/06/1999, Oct 1999
Location: Orlando, FL , USA
On page(s): 14-19
Oct 1999
References Cited: 4
IEEE Catalog Number: PR00465
Number of Pages: ix+110
INSPEC Accession Number: 6409772

Abstract:
The paper concerns a configurable soft core of the 8051 μC implemented VHDL. The main goal of efforts undertaken during design of the core was the compatibility with the industrial standards 80C51 and 80C52 on the instructi and timing levels. It doesn't limit flexibility of the core's architecture, which c easily optimized according to the current design constraints. The configuratio capabilities of the core are grouped in a configuration package. That approacl allows for separation from the indigenous part of the core, which remains untouched by a user and can be encoded in order to hide the VHDL code. Ins the configuration package there are several constants. Assigning values to th user has the opportunity to determine the core's structure (types of functiona modules used in the core), RAM and ROM sizes, the instruction set, number c interrupted sources, number of execution cycles for division and multiplicatio etc. The core is independent of the CPU peripheral modules (e.g. timer/count I/O ports, UART, etc.) due to a SFR bus. Peripherals are accessed by the use special function registers. The upper half of available addresses of the interna RAM is just reserved for them. Hence the communication between the CPU ar SFRs is carried out in the same way as in the case of memory cells. The core been proven on silicon. It was applied in the smart pressure sensor chip and 8031-compatible μC. The compatibility with the industrial was checked o logic verifier, where original 80C51 and 80C52 chips were applied during test references

Index Terms:
configuration management hardware description languages instruction sets microcontrollers standards 8031-compatible &mu C 8051 &mu C 80C51 80C52 peripheral modules ROM sizes SFR bus VHDL code configurable soft core configu capabilities configuration package design constraints execution cycles functional modules industrial standards instruction set internal RAM interrupted sources logic verifier reusable microcontroller core design smart pressure sensor chip special func registers timing levels

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L6: Entry 4 of 19 File: USPT Aug 27, 2002

DOCUMENT-IDENTIFIER: US 6442630 B1
TITLE: Electronic device that controls the vailidity of information based on a selected function unit

Detailed Description Text (66):
It is assumed that the electronic equipment of this embodiment having the structure shown in FIG. 7 operates as the digital moving image camera/recorder and communicates with another node by supplying node information onto the 1394 bus 13 via the 1394 serial bus I/F circuit 5, under the first subsidiary communication protocol stored in the first configuration ROM (CR1) 8.

Detailed Description Text (81):
The digital still image camera/recorder (second unit) is reconfigured and the C & S register 10 is set use with the digital still image camera/recorder. Next, in order to change the node information of the 1394 serial bus I/F circuit 5 from the first configuration ROM 8 to the second configuration ROM 9, the address setting of the I/F control and address conversion circuit 7 is changed. Namely, since the configuration ROMs 8 and 9 are located at different addresses in the above-described address space, the address setting is changed to select the second configuration ROM 9.

Detailed Description Text (82):
Thereafter, in order to reconfigure the management configuration of the 1394 serial bus 13 under the reset state, the bus interconnection of the 1394 serial bus I/F circuit 5 is recovered. In this manner, the electronic equipment of this embodiment is newly defined as the digital still image camera/recorder having the still image subsidiary communication protocol, in accordance with the new bus management configuration and the node information in the second configuration ROM 9. This new definition is detected by the root node which controls the bus management of the system shown in FIG. 5, and therefore recognized by the system.

Detailed Description Text (88):
If changed to the digital video (moving image camera/recorder), the flow advances to Step S4 to perform the unit control corresponding to the system configuration of the digital video, at Step S5 the C & S register 10 is set for use with the digital video, and at Step S6 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the first configuration ROM 8.

Detailed Description Text (89):
If it is judged at Step S3 that the equipment has been changed to the digital camera (still image camera/recorder), the flow advances to Step S7 to perform the unit control corresponding to the system configuration of the digital camera, at Step S8 the C & S register 10 is set for use with the digital camera, and at Step S9 the address setting of the I/F control and address conversion circuit 7 is changed in order to set the node information of the 1394 serial bus I/F circuit 5 to have the information stored in the second configuration ROM 9.

Detailed Description Text (90):
After the processes at Steps S4 to S6 or Steps S7 to S9, the reset state of the 1394 serial bus 13 started at Step S2 is released to recover the bus connection of the 1394 serial bus I/F circuit 5. At Step S11 the root node executes a new bus

management process after the system change and recognizes the equipment of this embodiment either as the moving image camera/recorder having the AV/C protocol or as the still image camera/recorder having the still image subsidiary communication protocol, in accordance with the contents of the configuration ROM 8 or 9.

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L6: Entry 4 of 19 File: USPT Aug 27, 2002

US-PAT-NO: 6442630
DOCUMENT-IDENTIFIER: US 6442630 B1

TITLE: Electronic device that controls the vailidity of information based on a selected function unit

DATE-ISSUED: August 27, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takayama; Nobutoshi	Yokohama			JP
Itou; Masamichi	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 10/ 020231 [PALM]
DATE FILED: December 18, 2001

PARENT-CASE:
This application is a division of application Ser. No. 09/614,547, filed Jul. 12, 2000, now U.S. Pat. No. 6,353,868, which is a division of application Ser. No. 09/414,319, filed Oct. 7, 1999, now U.S. Pat. No. 6,138,196, which is a division of application Ser. No. 08/917,295, filed Aug. 25, 1997, now U.S. Pat. No. 5,991,842.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-225183	August 27, 1996

INT-CL: [07] G06 F 13/00, G06 F 13/38

US-CL-ISSUED: 710/105; 710/100, 710/305
US-CL-CURRENT: 710/105; 710/100, 710/305

FIELD-OF-SEARCH: 710/105, 710/305, 710/314, 710/11, 710/100, 710/315, 711/100, 709/231, 348/22, 348/231, 725/147

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4499556	February 1985	Halpern	
☐	5329555	July 1994	Marko et al.	
☐	5506965	April 1996	Naoe	395/200
☐	5517647	May 1996	Kamada et al.	355/728
☐	5519832	May 1996	Warchol	395/183
☐	5691714	November 1997	Mehnert et al.	340/870
☐	5935208	August 1999	Duckwall et al.	709/221
☐	6038625	March 2000	Ogino et al.	710/104

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ABSTRACT:

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

9 Claims, 12 Drawing figures

L6: Entry 17 of 19 File: USPT Mar 16, 1999

DOCUMENT-IDENTIFIER: US 5883621 A
TITLE: Device control with topology map in a digital network

Detailed Description Text (18):
Returning to FIG. 3, step 408, after the self identification process, a device identification process is performed. During this process 408, DSS IRD 100 sends commands to all the nodes and inquires as to their respective device types. Device type information may be stored in and returned from a configuration ROM associated with each node of the serial bus as is known in the art.

WEST

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L6: Entry 17 of 19 File: USPT Mar 16, 1999

US-PAT-NO: 5883621
DOCUMENT-IDENTIFIER: US 5883621 A

TITLE: Device control with topology map in a digital network

DATE-ISSUED: March 16, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Iwamura; Ryuichi	San diego	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sony Corporation	Tokyo			JP	03
Sony Electronics, Inc.	Park Ridge	NJ			02

APPL-NO: 08/ 664445 [PALM]
DATE FILED: June 21, 1996

INT-CL: [06] G06 F 15/00

US-CL-ISSUED: 345/327; 345/339, 345/348, 345/969
US-CL-CURRENT: 725/37; 345/719, 345/735, 345/969, 725/131

FIELD-OF-SEARCH: 395/329, 395/339, 395/340, 395/342, 395/348, 395/349, 395/352, 395/356, 395/357, 395/970, 395/969, 345/329, 345/969, 345/970, 345/327, 345/339, 345/348, 345/356

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5021976	June 1991	Wexelblat et al.	345/356
☐	5226120	July 1993	Brown et al.	395/200.54
☐	5261044	November 1993	Dev et al.	345/348
☐	5353399	October 1994	Kuwamoto et al.	345/349
☐	5504863	April 1996	Yoshida	395/184.01
☐	5548722	August 1996	Jalalian et al.	395/200.5

OTHER PUBLICATIONS

Response to EIA R4.1 Committee Request for Proposals for Baseband Digital Interface,

Sony Corporation, Texas Instruments,Inc., Thursday, Aug. 31, 1995.
P1394 Standard for a High Performance Serial Bus, Copyright.sup..COPYRGT. 1995 by The Instutute of Electrical And Electronic Engineers, Inc., P 1394 Draft 8..0v3, Oct. 15, 1995.

ART-UNIT: 273

PRIMARY-EXAMINER: Huynh; BA

ABSTRACT:

A topology map for a digital system is generated and displayed on a display device to indicate the various components which make up the system. The various components are indicated using icons each of which represent a respective one of the components. A user specifies a source device and a receive device by manipulating the corresponding icons so as to cause a data transfer between the source device and the receive device. The data transfer may include the transfer of video data, audio data, or both. In a preferred embodiment, the digital network corresponds to the IEEE 1394 Serial Bus Standard.

15 Claims, 14 Drawing figures

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L6: Entry 18 of 19 File: USPT Sep 15, 1998

DOCUMENT-IDENTIFIER: US 5809331 A
TITLE: System for retrieving configuration information from node configuration memory identified by key field used as search criterion during retrieval

Abstract Text (1):
A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. Upon system initialization, the bus is scanned and device-specific identification information is retrieved from command and status configuration ROMs associated with each of the plurality of nodes. In one embodiment, a search routine is used to retrieve the device specific information. The search routine begins with the definition of an iterator which is used as a place holder during the search. A simple search begins at the root directory of a hierarchical tree data structure and continues until all directories within the tree have been searched. In more complex embodiments, search relationships (i.e., direction) parameters are defined. Search criteria such as node spec.sub.-- ID and software version numbers are specified and the search is commenced. The search continues until all matching device specific information entries have been returned. The device specific information can be used to load and configure associated drivers for nodes.

Detailed Description Text (14):
For an embodiment conforming to the IEEE 1394 Serial Bus Standard, each transaction capable node 12, 15, 16, 24, 32, 34, 40 and 44 of the serial bus implements a configuration ROM. The configuration ROM is a nonvolatile memory which stores critical boot information which is accessed during bus initialization as described below. The boot information is stored in the Name Registry and used to identify the appropriate driver software to be loaded for the node of interest.

Detailed Description Text (15):
FIG. 3 illustrates the general ROM format for each configuration ROM 50 of the serial bus. For one embodiment, the node configuration ROMs 50 reside within the address space of the serial bus in accordance with the IEEE 1394 Serial bus Standard. As shown, the configuration ROM 50 is divided into a root directory 52, various root dependent directories 54, root leafs 56, unit directories 58, unit dependent directories 60, and unit leafs 62. Thus, the directories are arranged in a hierarchical fashion. Within this structure, directories may have "children", "parents" and "siblings".

Detailed Description Text (17):
All directories in the node configuration ROMs 50 have the format shown in FIG. 4. The directory length parameter specifies the number of following quadlet entries in the directory. Each directory entry then has the format shown in FIG. 5. Each directory entry is broken down into a key field and an entry value field. The key field itself has two fields: the key type, indicating the type of directory entry, and the key value, specifying the particular directory entry, e.g., spec.sub.-- ID, unit software version, etc. The key type definitions for a preferred embodiment according to the IEEE 1394 Serial Bus Standard are shown in Table 1, below.

Detailed Description Text (18):
For an immediate entry, the entry value is the 24-bit value for that directory entry. Its meaning is dependent on the type of entry. For an offset entry, the entry value contains a 24-bit offset field. The offset value specifies a CSR address as a

quadlet offset from the base address of the initial register space. For the leaf and directory entries, the entry value provides a 24-bit indirect offset value which specifies the address of the leaf or directory of the indirect space. The indirect offset value indirectly specifies the ROM offset address of the leaf or the directory. Thus, using the key type and key value, a specific entry in the configuration ROM 50 of a node on the serial bus can be identified.

Detailed Description Text (19):
The present invention provides a method for searching the configuration ROMs 50 of the nodes on a serial bus. In one embodiment, a method of searching for and retrieving node software version and spec.sub.-- ID information is provided. This information can then be used by computer system 5 to load appropriate driver software for the nodes of the bus.

Detailed Description Text (20):
The search routine, in one embodiment, is provided with a pointer to the CSR configuration ROM of a specified node within the address space of the serial bus. Search parameters are defined. The search parameters correspond to the key types and key values defined for the node software version number and spec.sub.-- ID. Using these parameters, the search routine scans the address space of the configuration ROM and returns with matches for the given search parameters.

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L6: Entry 18 of 19 File: USPT Sep 15, 1998

US-PAT-NO: 5809331
DOCUMENT-IDENTIFIER: US 5809331 A

TITLE: System for retrieving configuration information from node configuration memory identified by key field used as search criterion during retrieval

DATE-ISSUED: September 15, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Staats; Erik P.	Brookdale	CA		
Lash; Robin D.	Milpitas	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Apple Computer, Inc.	Cupertino	CA			02

APPL-NO: 08/ 626462 [PALM]
DATE FILED: April 1, 1996

INT-CL: [06] G06 F 13/00, G06 F 13/24, G06 F 13/36

US-CL-ISSUED: 395/830; 395/500, 395/872, 395/284, 395/681
US-CL-CURRENT: 710/10; 703/22, 709/321, 710/104, 710/52

FIELD-OF-SEARCH: 395/651, 395/681, 395/872, 395/830, 395/500, 395/284

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4020466	April 1977	Cordi et al.	340/172.5
☐	5202986	April 1993	Nickel	395/600
☐	5343471	August 1994	Cassagnol	370/85.13
☐	5586268	December 1996	Chen et al.	395/250
☐	5598563	January 1997	Spies	395/652
☐	5630076	May 1997	Saulpaugh et al.	395/284
☐	5713009	January 1998	DeRosa, Jr. et al.	395/500

OTHER PUBLICATIONS

ISO/IEC 13213 ANSI/IEEE Standard 1212, "Information Technology--Microprocessor Systems--Control and Status Registers (CSR) Architecture For Microprocessor Buses", First Edition, pp. 1-125, (Oct. 5, 1994).
Philips Electronics et al, Digital Interface for Consumer Electronic Audio/Video Equipment Draft Version 2.0, IEEE 1394 Trade Association Meeting, pp. 1-47, Part 2--pp. 1-6, (Oct. 1995).
High Performance Serial Bus Working Group of the Microprocessor and Microcomputer Standards Committee, "P1394 Standard for a High Performance Serial Bus", P1394 Draft 8.0v3, pp. 1-364, (Oct. 16, 1995).
Apple Computer, "Inside Macintosh, Devices", Nov. 1994, pp. 3.1-3.48.
"Information Technology--Microprocessor Systems--Control and Status Registers (CSR) Artchitecture for Microcomputer Buses" IEEE 1212, 1994.
"Standard for a High Performance Serial Bus", IEEE 1394, Oct. 1995, pp. ii-364.
Apple Computer, "Designing PCI Cards and Drivers for Power Macintosh Computers", Mar. 1995, pp. 1-366.
Apple Computer, Inc., "Interim Draft, Designing PCI Cards and Drivers for Power Macintosh Computers", A8 Draft--Preliminary Information, pp. 1-372, (Mar. 9, 1995).

ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Perveen; Rehana

ABSTRACT:

A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. Upon system initialization, the bus is scanned and device-specific identification information is retrieved from command and status configuration ROMs associated with each of the plurality of nodes. In one embodiment, a search routine is used to retrieve the device specific information. The search routine begins with the definition of an iterator which is used as a place holder during the search. A simple search begins at the root directory of a hierarchical tree data structure and continues until all directories within the tree have been searched. In more complex embodiments, search relationships (i.e., direction) parameters are defined. Search criteria such as node spec.sub.-- ID and software version numbers are specified and the search is commenced. The search continues until all matching device specific information entries have been returned. The device specific information can be used to load and configure associated drivers for nodes.

12 Claims, 6 Drawing figures

(12) **United States Patent**
Snyder

(10) **Patent No.: US 6,370,635 B2**
(45) **Date of Patent: *Apr. 9, 2002**

(54) **DUAL ROM MICROPROGRAMMABLE MICROCONTROLLER AND UNIVERSAL SERIAL BUS MICROCONTROLLER DEVELOPMENT SYSTEM**

(75) Inventor: **Warren S. Snyder**, Snohomish, WA (US)

(73) Assignee: **Cypress Semiconductor Corp.**, San Jose, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/481,038**

(22) Filed: **Jan. 11, 2000**

Related U.S. Application Data

(63) Continuation of application No. 09/189,216, filed on Nov. 10, 1998, now abandoned, which is a continuation of application No. 08/705,807, filed on Aug. 30, 1996, now Pat. No. 5,859,993.

(51) **Int. Cl.**[7] **G06F 9/30**
(52) **U.S. Cl.** **712/32**
(58) **Field of Search** 712/208, 239, 712/32

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(74) *Attorney, Agent, or Firm*—Christopher P. Maiorana, P.C.

(57) **ABSTRACT**

A microprogrammable microprocessor that stores microprogramming instruction sets in a dual ROM configuration enhancing reusability of subroutine operations common between two or more instructions. A first ROM contains a look up table identifying the subroutine(s) utilized by each instruction. The second ROM contains the subroutines needed to implement the required operations for each instruction. The dual ROM microprogrammable microprocessor is used in a Universal Serial Bus microcontroller development system having a microprocessor, control circuit, and an interface to USB bus. The microprocessor system state and I/O registers are mapped to a system bus sharing the same lines with a control circuit. The control circuit provides an RS-232 interface to an attached computing device able to write and read data words to the system bus, thereby to control the microprocessor and associated hardware by setting the system state and writing/reading data from RAM. The control circuit is also attached to a Universal Serial Bus, hence allowing 100% testing of USB compliant devices and firmware. The circuit specs can be programmed in a Hardware Description Language which is

US006138196A

United States Patent [19]

Takayama et al.

[11] Patent Number: 6,138,196

[45] Date of Patent: Oct. 24, 2000

[54] **COMMUNICATION SYSTEM FOR PROVIDING DIGITAL DATA TRANSFER, ELECTRONIC EQUIPMENT FOR TRANSFERRING DATA USING THE COMMUNICATION SYSTEM, AND AN INTERFACE CONTROL DEVICE**

[75] Inventors: **Nobutoshi Takayama**, Yokohama; **Masamichi Itou**, Tokyo, both of Japan

[73] Assignee: **Canon Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **09/414,319**

[22] Filed: **Oct. 7, 1999**

Related U.S. Application Data

[62] Division of application No. 08/917,295, Aug. 25, 1997, Pat. No. 5,991,842.

[30] **Foreign Application Priority Data**

Aug. 27, 1996 [JP] Japan 8-225183

[51] **Int. Cl.**[7] **G06F 13/00**; G06F 13/42

[52] **U.S. Cl.** **710/105**; 710/104; 710/106; 710/11; 710/62

[58] **Field of Search** 710/105, 104, 710/106, 11, 62, 101, 129; 709/238, 253; 370/463, 912; 379/88.13

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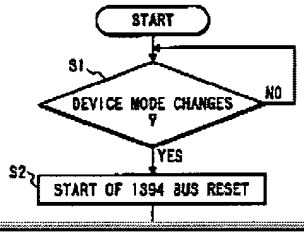
Attorney, Agent, or Firm—Fitzpatrick, Cella, Harper & Scinto

[57] **ABSTRACT**

An electronic equipment for communications with other nodes via a serial bus interface. The electronic equipment has a plurality of functions, and stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, communications suitable for each function can be executed via the serial bus interface. An interface control device used with an electronic equipment having a plurality of functions stores a plurality piece of information representative of the plurality of functions. The communication system selectively reads the stored information and realizes the function corresponding to the read information. Accordingly, the electronic equipment can perform communications suitable for each function.

11 Claims, 10 Drawing Sheets



US005809331A

United States Patent [19]

Staats et al.

[11] **Patent Number: 5,809,331**

[45] **Date of Patent: Sep. 15, 1998**

[54] **SYSTEM FOR RETRIEVING CONFIGURATION INFORMATION FROM NODE CONFIGURATION MEMORY IDENTIFIED BY KEY FIELD USED AS SEARCH CRITERION DURING RETRIEVAL**

[75] Inventors: **Erik P. Staats**, Brookdale; **Robin D. Lash**, Milpitas, both of Calif.

[73] Assignee: **Apple Computer, Inc.**, Cupertino, Calif.

[21] Appl. No.: **626,462**

[22] Filed: **Apr. 1, 1996**

[51] **Int. Cl.**[6] **G06F 13/00**; G06F 13/24; G06F 13/36

[52] **U.S. Cl.** **395/830**; 395/500; 395/872; 395/284; 395/681

[58] **Field of Search** 395/651, 681, 395/872, 830, 500, 284

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Assistant Examiner—Rehana Perveen
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A computer system comprises a plurality of nodes interconnected by point-to-point links and forms a serial bus. Upon system initialization, the bus is scanned and device-specific identification information is retrieved from command and status configuration ROMs associated with each of the plurality of nodes. In one embodiment, a search routine is used to retrieve the device specific information. The search routine begins with the definition of an iterator which is used as a place holder during the search. A simple search begins at the root directory of a hierarchical tree data structure and continues until all directories within the tree have been searched. In more complex embodiments, search relationships (i.e., direction) parameters are defined. Search criteria such as node spec_ID and software version numbers are specified and the search is commenced. The search continues until all matching device specific information entries have been returned. The device specific information can be used to load and configure associated drivers for nodes.

12 Claims, 4 Drawing Sheets